IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

pplicant(s): Kimoto

al No.: 09/850,254

Filed: May 7, 2001

Title: Semiconductor

Apparatus

Manufacturing Method Therefor

Attorney Docket No.: N13476100S

Group Art Unit: 2826

Examiner: Quinto, K.

RESPONSE TO OFFICE ACTION

and

Assistant Commissioner for Patents Washington, D.C. 20231

Dear Sir:

The following is submitted in response to the Office Action dated December 4, 2001, and is currently due January 4, 2002.

REMARKS

Election without Traverse

In response to the restriction requirement set forth in the Office Action dated December 4, 2001, the claims of Group I (claims 1-13) are elected without traverse.

Respectfully Submitted.

Attorney

Reg. No. 43,232

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37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Typed Name: Darryl G. Walker